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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/820,026	04/08/2004	Hiroyuki Nagamori	HITA.0534	7585

7590 08/16/2005

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EXAMINER	
LE, DINH THANH	
ART UNIT	**PAPER NUMBER**
2816	

DATE MAILED: 08/16/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/820,026	NAGAMORI ET AL	
	Examiner	Art Unit	
	DINH T. LE	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-13 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-2, 5-9 and 11-13 is/are rejected.

7)☒ Claim(s) 3,4 and 10 is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☒ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 4/8/04.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Specification

The specification has been checked to the extent necessary to determine the presence of all possible minor errors. However, the applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Rejections

Claim Rejections - 35 USC § 112

Claims 5-6, 8-9 and 11-13 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Correction or clarification is required.

In claim 5, it is unclear how the bias circuit can give a bias to the amplification circuit. The description of the present invention is incomplete because the bias circuit is not connected to anything. Thus, the claimed bias circuit may not perform the recited function. The same is true for claim 10.

In claim 6, the recitation "said first transistor" on line 4 and "such a bias" on line 3 lacks clear antecedent basis. It is not understood where the "first transistor" comes from, how the voltage can bias the first transistor to perform a class B and how this limitation is read on the preferred embodiment or seen on the drawings.

In claim 8, it is unclear how signal can "enable feedback control", where the feedback control comes from and how the citation "transistor" on line 5, "first transistor", "second transistor", "third transistor", "fourth transistor", "a current detection circuit having a transistor

for output detection which receives an input signal" on lines 5-6 and "said component outputting a signal for enabling feedback control" on lines 12-13 is read on the preferred embodiment. Insofar as understood, no such limitation is seen on the drawings.

In claim 9, the recitation "voltage" on line 7 is confusing because it is unclear if this is additional "voltage" or further recitation of previously claimed "voltage" on line 6. The same is true for reciting "high frequency power amplification" on line 10, "output power" on line 16 in claim 11, "output power" on line 13 of claim 12, and "signal" on line 7 of claim 13.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-2 and 5 are rejected under 35 USC 102 (b) as being anticipated by Ishikawa et al (US 5,982,236).

Ishikawa et al discloses in Figure 1 a power amplifier circuit comprising:

- amplifier stages (TR2);
- an output power detection circuit (4) for detecting a magnitude of an output power of the power amplification circuit and outputting a signal to the gate of a transistor (Tr2) for enabling feedback control of the output power of said power amplification circuit; and
- wherein said output power detection circuit (4) receives a monitor voltage from an impedance matching circuit (3) provided closer to an output of said power amplification circuit via a capacitor element (C12) and detects the output power amplification circuit.

With regard to claim 2, the recitation "resistor" is read on the resistor (R11) as shown in Figure 1.

With regard to claim 5, the recitation "bias circuit" is read on elements (S4, VDD2, S4).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-2, 5 and 7 are rejected under 35 USC 103 (a) as being unpatentable over Chen et al (US 2002/0137481, S/N=09/855,511) in view of Ishikawa (US 6,982,236).

Chen et al discloses in Figure 2 a power amplifier circuit comprising:

- amplifier stages (21-23);
- an output power detection circuit (41-43) for detecting a magnitude of an output power of the power amplification circuit and outputting a signal to the amplifiers (21-23) for enabling feedback control of the output power of said power amplification circuit; and
- wherein said output power detection circuit (41-43) receives a monitor voltage from an impedance matching circuit (31-33) provided closer to an output of said power amplification circuit.

However, Chen et al does not discloses that the detection circuit comprising a capacitor element and a resistor.

Ishikawa suggests in Figure 1 a power amplifier comprising a capacitor (C12) and a resistor (R11) for eliminating DC current components, see lines 65-67, column 11.

It would have been obvious to a person having skill in the art at the time the invention was made to employ the resistor and the capacitor suggested by Ishikawa in the Chen circuit for the purpose of eliminating DC current component.

With regard to claim 5,the recitation "bias circuit" is read on the element (51).

With regard to claim 7, implementing the power amplifier on an IC for reducing size is well known in the art. Lacking of showing any criticality, it would have been obvious to a person having skill in the art at the time the invention was made to implement the modified power amplifier circuit of Chen et al on an IC for the purpose of reducing size.

Allowable Subject Matter

Claims 3-4, 6 and 8-13 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, second paragraph, set forth in this Office action and/or to include all of the limitations of the base claim and any intervening claims.

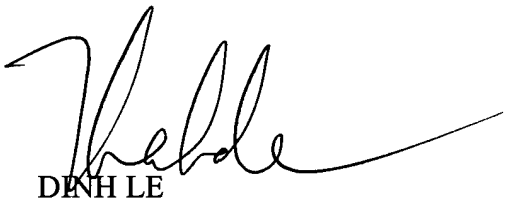
The claims are allowed because the prior art of record does not show the matching circuit as combined in claim 3, the detection circuit comprising transistors and substraction circuit as combined in claim 4, the low pass filter as combined in claim 9 and the output level control circuit as combined in claim 11.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to DINH T. LE whose telephone number is (571) 272-1745. The examiner can normally be reached on Monday-Friday (8AM-7PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, TIMOTHY CALLAHAN can be reached at (571) 272-1740.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



DINH LE
Primary Examiner